REMARKS

I. Introduction

Claims 16 and 20 have been canceled. Claims 36 and 37 have been added. Claims 12 to 15, 17 to 19, and 21 to 37 are pending in the present application. In view of the foregoing amendments and the following remarks, it is respectfully submitted that all of the presently pending claims are allowable, and reconsideration is respectfully requested.

II. Claim Objection

While Applicants do not agree with the merits of the objection to claim 14, to facilitate matters, claim 14 has been amended to obviate the objection. Accordingly, withdrawal of this objection is respectfully requested.

III. Rejection of Claims 12 to 35 Under 35 U.S.C. § 103(a)

Claims 12 to 35 were rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of U.S. Patent No. 5,802,290 ("Casselman"), U.S. Patent No. 5,889,982 ("Rogers"), and U.S. Pat. No. 4,682,284 ("Schrofer"). It is respectfully submitted that the proposed combination of Casselman, Rogers, and Schrofer does not render unpatentable claims 12 to 35 at least for the following reasons.

To establish a prima facie case of obviousness, the Office Action must demonstrate three criteria: (1) there must be some suggestion or motivation to one of ordinary skill in the art to modify a reference or to combine reference teachings; (2) there must be a reasonable expectation of success; and (3) the prior art reference (or references when combined) must teach or suggest each and every limitation in the claim under examination. In re Vaeck, 947 F.2d 488 (Fed. Cir. 1991).

Claim 12 recites a system for reconfiguring a programmable unit, the programmable unit including a plurality of reconfigurable function cells in a multidimensional arrangement. The claimed system includes

> *a primary logic unit in communication with at least one of the plurality of reconfigurable function cells, the primary logic unit configured to detect an event and to detect a state of the at least one of the plurality of reconfigurable function cells.*

Claim 12, as herein amended without prejudice, further recites:

> *a FIFO memory shared by the plurality of reconfigurable function cells and coupled to the primary logic unit configured to store a plurality of configuration*

data associated with the plurality of reconfigurable function cells, the plurality of configuration data including the first configuration data.

Claim 18 recites a method for reconfiguring a programmable unit, the programmable unit including a plurality of reconfigurable function cells in a multidimensional arrangement. The claimed method includes

detecting an event and a state of at least one of the plurality of reconfigurable function cells.

Claim 18, as herein amended without prejudice, further recites:

storing, in a FIFO memory shared by the plurality of reconfigurable function cells, a plurality of configuration data associated with the plurality of reconfigurable function cells, that includes the first configuration data.

Claim 25 recites a system for run-time reconfiguration of a programmable unit, the programmable unit including a plurality of reconfigurable function cells in a multidimensional arrangement. The claimed system includes

a primary logic unit in communication with at least one of the plurality of reconfigurable function cells, the primary logic unit configured to detect an event and to detect a state of the at least one of the plurality of reconfigurable function cells.

Claim 25, as herein amended without prejudice, further recites:

a FIFO memory shared by the plurality of reconfigurable function cells and coupled to the primary logic unit configured to store a plurality of configuration data associated with the plurality of reconfigurable function cells, the plurality of configuration data including the first configuration data, the first configuration data stored in the FIFO memory if the selected one of the plurality of reconfigurable function cells is not in a reconfiguration state, and the primary logic unit configured to reconfigure the selected one of the plurality of reconfigurable function cells if the selected one of the plurality of reconfigurable function cells is in a reconfigurable state.

The Examiner alleges that Casselman discloses the recited plurality of reconfigurable function cells to be configured by configuration data. The Examiner further alleges that Schrofer discloses the recited FIFO memory. However, as set forth in Applicants' response, dated January 30, 2004, neither Schrofer, nor Rogers, nor Casselman, nor their combination teach or suggest that configuration data from multiple functional units is stored in a shared FIFO memory. The Examiner, in the "Response to Arguments," asserts that "Applicant has not specifically claimed a common or shared FIFO." As an initial matter, claims 12 and 25 recite "a FIFO memory . . . configured to store a plurality of configuration data **associated with *the plurality of reconfigurable function cells***, and claim 18 recites "storing, in a FIFO memory . . . a plurality of configuration data **associated with *the plurality of reconfigurable function cells***."

Thus, the claims recite that configuration data of more than one reconfigurable function cell is stored in a particular FIFO memory. Furthermore, claims 12, 18, and 25 have been amended herein without prejudice to recite that the FIFO memory is "shared by the plurality of reconfigurable function cells."

Furthermore, claim 12 recites a primary logic unit configured to detect a state of the at least one function cell; claim 18 recites detecting a state of the at least one function cell; and claim 25 recites a primary logic unit configured to detect a state of the at least one function cell, and that on the basis of a detected state, either a function cell is reconfigured or otherwise a configuration data is stored in a FIFO memory. The Examiner asserts that Casselman, in Figure 5, at column 3, lines 14 to 21, and at column 4, lines 35 to 46, discloses the recited detection of a state of the at least one function cell. However, while Casselman may refer to a reconfigurable computation array 20 under the control of a reconfigurable control section 21 that may receive communications from a host 12, nowhere does Casselman disclose or suggest that the host 12 detects a state of either the reconfigurable control section 21 or the reconfigurable computation array 20, or that the reconfigurable control section 21 detects a state of the reconfigurable computation array 20. Indeed, neither Schrofer, nor Rogers, nor Casselman, nor their combination teach or suggest a primary logic unit that detects a state of the at least one function cell.

Thus, because none of the cited references teach or suggest the recited limitations, and in particular the notions of having reconfiguration data from multiple cells stored on a shared FIFO, and of detecting a state of a function cell, the suggested combination of Casselman, Rogers, and Schrofer does not teach or suggest each and every limitation in claims 12, 18, and 25 and thus claims 12, 18, and 25 should not be obvious over the cited references.

Furthermore, the Examiner alleges that it would have been obvious to include Schrofer's FIFO memory in the invention of Casselman. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680 (Fed. Cir. 1990). The Examiner states that the desirability of the combination is to be able to queue up configuration data to a configurable cell even when the cell is not in a configurable state.

However, Applicants respectfully submit that none of the cited references teaches or suggests the notion of using a shared FIFO queue for multiple functional units in a multiprocessor as recited in Applicants' claims 12, 18, and 25, or of combining a FIFO queue with some other elements to achieve this result. Simply desiring to queue up requests for a processor is not a motivation to make the combination proposed by the Examiner in a way that results in Applicants' claims 12, 18, and 25, where the queue is shared by multiple cells. In Applicants' claimed system and method, a purpose of the shared queue is to cause other cells to wait for the completion of processing at a given cell. This is most conveniently achieved using the claimed shared FIFO queue. Thus, none of the cited references teach or suggest the Examiner's proposed combination.

Thus, for at least the reasons given above, the suggested combination of Casselman, Rogers, and Schrofer does not render unpatentable claims 12, 18, and 25.

As for claims 13 to 15, and 17, which ultimately depend from claim 12 and therefore include all of the limitations of claim 12, it is respectfully submitted that the combination of Casselman, Rogers, and Schrofer does not render unpatentable claims 13 to 15, and 17 for at least the same reasons given above in support of the patentability of claim 12.

As for claims 19, and 21 to 24, which ultimately depend from claim 18 and therefore include all of the limitations of claim 18, it is respectfully submitted that the combination of Casselman, Rogers, and Schrofer does not render unpatentable claims 19, and 21 to 24 for at least the same reasons given above in support of the patentability of claim 18.

As for claims 26 to 35, which depend from claim 25 and therefore include all of the limitations of claim 25, it is respectfully submitted that the combination of Casselman, Rogers, and Schrofer does not render unpatentable claims 26 to 35 for at least the same reasons given above in support of the patentability of claim 25.

IV. New Claims 36 and 37

New claims 36 and 37 have been added herein. It is respectfully submitted that new claims 36 and 37 do not add any new matter and are fully supported by the present application, including the Specification. Since new claim 36 recites "wherein the primary logic unit is configured to ***check a reconfigurability state*** of the

selected one of the plurality of function cells before reconfiguring the selected one of the plurality of function cells," it is respectfully submitted that claim 36 is patentable over the references relied upon for at least the same reasons set forth above in support of the patentability of claim 25. Since new claim 37 recites "a FIFO memory ***shared by the plurality of reconfigurable function cells*** and that stores configuration data associated with the plurality of reconfigurable function cells," it is respectfully submitted that claim 37 is patentable over the references relied upon for at least the same reasons set forth above in support of the patentability of claim 25.

V. Conclusion

Applicants respectfully submit that all of the pending claims of the present application are in condition for allowance. Prompt reconsideration and allowance of the present application are therefore earnestly solicited.

Respectfully submitted,
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